A LOW-POWER FRONT-END MODULE DEDICATED TO WIRELESS CORTICAL DATA RECORDING

Benoit Gosselin, Virginie Simard, Jean-François Roy and Mohamad Sawan
PolySTIM Neurotechnologies Laboratory
École Polytechnique de Montréal, Electrical Engineering Department
benoit.gosselin@polymtl.ca

Abstract

This paper reports on the design and the implementation of a fully implantable cortical signals acquisition system. The pre-processing stage, one of the main modules, has been designed in CMOS 0.18um process and sent for fabrication. It includes a low-noise multichannel front-end and a new prototype analog wavelet processor intended for on-line neural signal detection. Ultra low power consumption is achieved for both modules with usage of CMOS weakly inverted transistors. Special attention has been paid on recording quality in the front-end design by using Chopper modulation technique. The proposed front-end achieves an input referred noise of less than 30nV/√Hz and its power consumption is below 20μW per channel. Custom object oriented software has also been implemented for neural data visualisation, storage and analysis, and for system configuration.

1. Introduction

Multielectrodes neural recording is becoming a prolific research paradigm in neurosciences. Since a few years, researchers have exploited the capabilities of micromachining and microelectronics to build heterogeneous devices that increase the number of recording sites and enhance acquisition quality. Electronic circuits needed for signal conditioning and data transmission have been combined with an implantable transducer following various techniques. Reliable acquisition devices have been designed based on this approach and used for chronic experiments. The frequent developments in this area and the degree of maturity reached by these microsystems allow hoping that they will be widely available and used on a permanent basis sooner than expected. Radio Frequency (RF) power and data transmission is a well suited solution for implantable devices. It avoids percutaneous hard wires connections which reliability is poor and which may induce infections. On-chip analog-to digital conversion, required to simplify wireless data transfer, increases signal-to-noise ratio (SNR) and enhances the bandwidth. Although experiments have succeed to control robotized members or communication software with a few dozens of cells [1], having more recording channels would increase the spatial resolution of measurements. Thus, on-chip event detection appears to be a good solution for bandwidth enhancement. Since most known neural data processing methods like spike sorting require complex software implemented algorithms, it is necessary to transmit raw spikes for further software processing. Low-power analog processing as wavelet transform and detection circuits would then be of great help for such an approach. The objective of our work is to design and implement an autonomous and reliable multichannel cortical recording system suitable for permanent implantation. The implantable recording device is powered and communicates wirelessly. An overview of the intended system is given in the next section, then the key elements of the system, namely the analog front-end, the prototype analog wavelet processor and the RF data link, are detailed in subsequent sections, followed by our results and a description of the implementation.

2. System overview

We chose to assemble the embedded integrated circuit (IC) with the microprobe using flip chip technique, giving more flexibility in the design and implementation of both parts. The front-end includes complete analog conditioning circuitry for each channel. The numerous channels are multiplexed and digitized for further wireless data transmission through an inductively coupled link established between the implanted device and an external controller. The transmitted data are then fed to a PC for software data processing and storage. Fig. 1 shows a block diagram of an implantable multichannel monitoring device.

3. Design description

3.1 The analog front-end

Input noise, power consumption and small integration surface are major concerns when designing implantable circuitry for such an application.

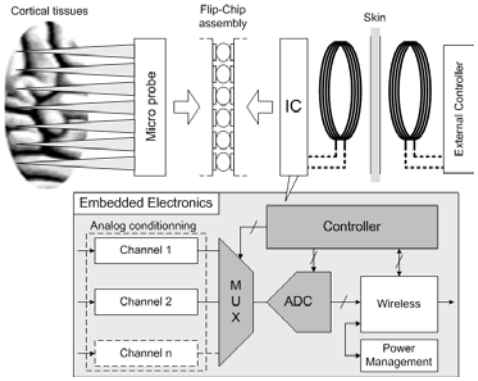

Figure 1. Block diagram of the device.

Low amplitude neural signals (1-100μV) are very sensitive to noise. Thus, special care must be put on the input noise level of the first and critical stage of the conditioning chain, mainly the preamplifier. Dominant noise sources in CMOS amplifiers are thermal noise and 1/*f* noise. The thermal noise in MOS transistors is directly related to the DC bias current of the transistors. Thus increasing the supplied current will generally lower the thermal noise floor. 1/*f* noise decreases almost linearly until it reaches the thermal noise floor at the corner frequency of the amplifier. A well known approach to decrease the 1/*f* noise level is to increase width (W) and length (L) of the amplifier's input transistors. This approach will usually make the preamplifier to dominate the entire integration area. The proposed front-end mitigates this trade-off with Chopper modulation technique [2]. Chopper modulation is an active method for low frequency noise (1/*f* noise) reduction. Consequently, as it will be shown later, the size of the preamplifier's transistors can be decreased considerably. As shown in fig. 2, each channel of the front-end includes a low-power Chopper amplifier. The chopper amplifiers are composed of an input modulator, a low-noise preamplifier, a 2nd order bandpass filter, a demodulator and a lowpass filter. A gain amplifier then reamplifies the neural signal sufficiently. The chopper frequency (f_{chop}) has been set to 20kHz.

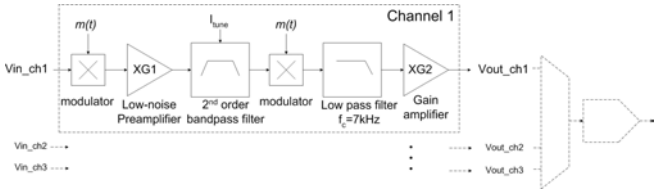

Figure 2. The analog front-end.

3.1.1 The low-noise preamplifier

Fig. 3 shows a schematic of the fully differential buffered transconductor used as preamplifier. The input transconductor formed by *M1-M6* operates in strong inversion to achieve low input noise level, while the output common drain buffers formed by *M9-M14* operate in weak inversion. The bias current *Ibi*, is set to 10μA giving drain current of 5μA to *M1–M6*. *Ibo*, set to 100nA, biases the output buffer. The preamplifier provides 40dB signal amplification.

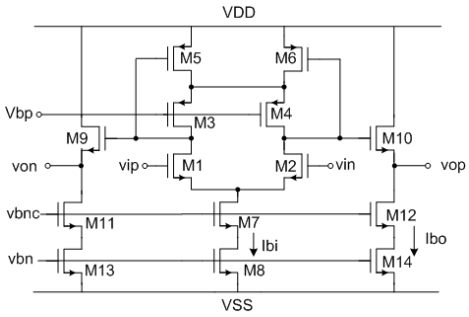

Figure 3. Low-noise preamplifier.

3.1.2 The low-power filters

A 2nd order Gm-C filter (fig. 4.) is used to implement the selective transfer function needed for optimum offset reduction in the chopper modulated front-end [2]. All transistors of the filter operate in the weak inversion region, allowing very small power consumption for this module. Small bias currents as a few nano amperes are used. The filter implements a bandpass transfer function when the output is taken from V_{o1} and a lowpass transfer function when the output is taken from V_{o2}. The filter uses a novel multiple input transconductors (G_{m1}) to reduce circuits complexity and sub-circuits interdependencies.

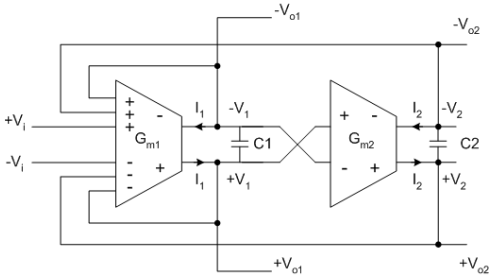

Figure 4. The 2nd order Gm-C filter.

3.1.3 The gain amplifier

A gain amplifier common to all channels would have been too much power consuming in order to meet the large bandwidth requirement. Consequently, an individual open loop Operational Transconductance Amplifier (fig. 5) is providing a final 40dB gain to the neural signal of each channel, prior to multiplexing and digitization.

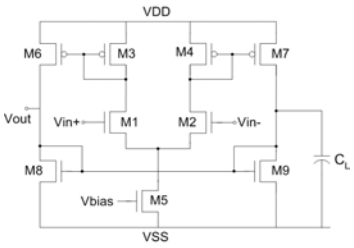

Figure 5. The gain amplifier.

3.2 Analog wavelet transform

As discussed in introduction, a special effort is put to increase the number of channels that can be sent over a RF data link, by means of event detection and eventually, data compression. One avenue that has been explored in order to facilitate these two steps is the application of wavelet transform to neural signals. The wavelet transform is a multiresolution analysis that is localized both in time and scale (that corresponds to frequency). One of its interesting properties is that it concentrates the signal energy into a few output coefficients that represent the useful part of the signal. The other very small coefficients may be considered as noise; they are removed using a threshold. Spike detection and compression are more efficient on this denoised transformed signal [3]. The wavelet transform is most often performed by means of digital filters that are very power and area consuming and thus hardly suitable for an implantable device. An analog implementation has then been chosen to reduce the power consumption. The analog wavelet processor is made up of a bandpass parallel filter bank of which the impulse response, that is, the wavelet itself, is a gaussian function. The filter bank covers the neural signal bandwidth (100Hz to 6kHz) and the center frequencies are logarithmically spaced, as shown on fig. 6a). Fig. 6b) shows the impulse responses of the filter bank.

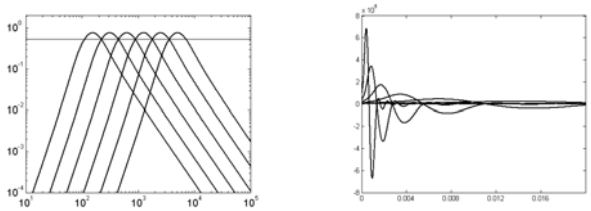

Figure 6. a) Frequency responses b) Impulse responses.

The gaussian function has been approximated by a sixth-order filter. To optimize the area of implementation, each 6th order filter is composed of three 2nd order filters in parallel and shares one on these filters with the next 6th order filter, leading to 13 2nd order filters for the whole wavelet processor, as illustrated on Fig. 7.

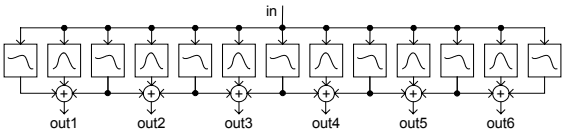

Figure 7. Parallel implementation of the filter bank.

The filters have been implemented using log-domain techniques: a design method taking advantage of the exponential relationship $I=f(e^{V})$ specific to bipolar transistors as well as weakly inverted CMOS transistors. Log-domain filters are current-mode; while their input/output signals are currents, their internal state variables are voltages that are an exponentially-compressed representation of the inputs. This characteristic, called companding, ensures a large dynamic range, which is needed for low-voltage systems [4]. All filter transistors are biased in weak inversion allowing a very low power dissipation. The second-order filter used consumes only 3μW.

3.3 RF data link

Load Shift Keying (LSK) modulation is used for neural data transfer, following analog conditioning and digitization. Configurations and commands are sent to the implanted system with OOK (ASK with a modulation index of 100%) modulation. A 13.56MHz carrier frequency, which is suitable for medical applications, is used. The monolithic RF data link uses half duplex data transfer. The electromagnetic energy is recovered from the 13.56MHz carrier with a voltage rectifier feeding a regulator with the received power to supply all modules in the implant. The block diagram of this module is shown on Fig. 8.

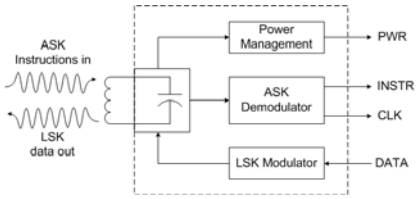

Figure 8. Block diagram of the wireless module.

3.4 Acquisition software

The transmitted neural data must be fed to a PC after demodulation for data storage and analysis. The acquired data are transferred from the external transceiver through a USB connection. USB provides fast transfer and enables the external system to be very portable. USB allows 32 channels with 30khz sampling rate per port. A standard PC may have as much as 2 or 3 USB ports. Multiport data transfer is supported by the software. The data transfer may then be distributed over a few USB ports to increase the

throughput. The software under development enables multiport data transfer, data reconstruction and data storage. The neural data can be saved to ASCII format or to Matlab format for further processing and analysis, such as spike sorting. Just as event detection and compression, spike sorting can beneficiate from the use of wavelet transform that emphasizes the difference between signals [5]. This mapping is depicted on fig. 9.

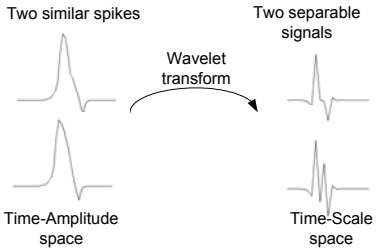

Figure 9. Illustration of the wavelet transform mapping.

4. Implementation and results

Tables 1, 2, 3and 4 summarize the main characteristics of the analog front-end modules.

Table 1. Preamplifier characteristics	
Parameters	Values
Supply voltage	1.8V
DC Gain	42.1 dB
Unity gain bandwidth	10.23MHz
Phase margin	50.1
Corner frequency	10kHz
Total input noise	25 nV/√Hz
PSRR	>100dB
CMRR	>110dB
Power consumption	18uW
Bias current	10uA
Input transistors (M1-M2) size	100/10u
Table 2. Bandpass filter characteristics	
Supply voltage	0.9V
THD	<1%
Power consumption	288nW
Supply current	319.8nA
Parameters	Values

Table 3. Gain amplifier	
Parameters	Values
DC gain	40.2 dB
Bandwidth	30.2kHz
Unity gain bandwidth	3.1MHz
Phase margin	77.3
Supply voltage	0.9V
Supply current	810nA
Power consumption	730nW
Compensation capacitor	500fF
Table 4. Overall system Summary	
Power consumption	<20uW
I/f noise attenuation (1-20kHz)	70-20dB
Input offset voltage	<0.1uV
Bandwidth	DC - 7kHz
Total gain	80 dB
Integration area	0.0705mm²

Fig. 10.a) shows a low input signal with additive noise, 10.b)-c) show Chopper modulation efficiency to reduce different 1/*f* noise levels induced in the preamplifier. One channel of the front-end has been implemented in CMOS 0.18μm process. As explained in section 1, Chopper modulation allows a smaller implementation for the preamplifier. As shown in Table 5, the presented preamplifier is smaller than other implementations. The monolithic RF data link exhibits a maximum bit rate of 1.507Mbps with ASK modulation. The LSK modulation achieves a bit rate of 1.13Mbps for neural data transfer.

Table 5. Size of Neural preamplifiers					
Source	Type	Area	Input Noise	Power Consump.	Process
R. Harrison (JSSC 2003)	PMOS	0.22 mm²	2.2uVrms	80uW	CMOS 1.5um
P. Mohseni, K. Najafi (EMBS/BEMS 2002)	PMOS	0.107 mm²	-	133uW	CMOS 1.5um
R. Olsson, K. Wise (EMBS 2003)	PMOS	0.082 mm²	16.6uVrms	92 uW	CMOS 3.0um
Andersen & al. (Trans. On Neur. Sys. & Rehab. 2003)	PMOS	-	2.5uVrms	240uW	CMOS 0.5um
This Work	**NMOS**	**0.015 mm2**	**2.5uVrms**	**20uW**	**CMOS 0.18um**

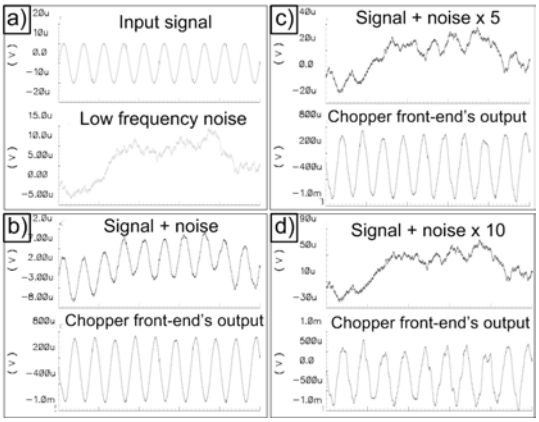

Figure 10. Chopper stabilized front-end performances.

5. Conclusion

The presented low-power implantable circuits are suitable for a neural data acquisition system. The principal design constraints that have been addressed are the maximisation of the number of channels versus wireless link bandwidth and the very low power consumption needed by implantable devices. The results show the low-power and low-noise characteristics of the implemented modules and the advantages gain from using Chopper modulation in the front-end have been demonstrated.

Acknowledgements

The authors would like to acknowledge the financial support from the National Sciences and Engineering Research Council of Canada (NSERC) and the design tools and fabrication resources from the Canadian Microelectronics Corporation (CMC).

References

[1] Taylor DM, Tillery SI, Schwartz AB, "Direct cortical control of 3D", *Neuroprosthetic devices*. *Science* 2002, 296:1829-1832.

[2] B. Gosselin, V. Simard, M. Sawan,"An Ultra Low-Power Chopper Stabilized Front-End For Multichannel Cortical Signals Recording", IEEE CCECE 2004.

[3] V. J. Samar, A. Bopardikar, R. Rao, K. Swartz,"Wavelet Analysis of Neuroelectric Waveforms: A Conceptual Tutorial," Brain and Language 66, pp. 7-60, 1999.

[4] D. Masmoudi, W. Serdijn, J. Mulder, A. Van Der Woerd, J. Tomas, J. P. Dom, "A new current mode synthesis method for dynamic translinear filters and its application in hearing aids," IEEE Conf. on Electronics, Circuits and Systems, vol. 2, pp. 337-340, 1998.

[5] J. C. Letelier, P. P. Weber, "Spike Sorting Based on Discrete Wavelet Transform Coefficients," J. Neurosci Meth. 101, pp. 93-106, 2000.